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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,576	11/12/2003	Tongbi Jiang	2269-4886.1US (01-0201.01	6662

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,576	JIANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/1/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 30 January 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,977,640 to Bertin et al.

Regarding claims 1, 5, and 6, Bertin discloses a method for assembling a multi-die package comprising: providing an interposer (32 in figs. 6-7 and 11-13; 88 in figs. 14-16) with a substantially planar surface and a receptacle formed substantially through the substrate (opening

containing die 40 in figs. 6-7, containing die 130 in figs. 12-13, and containing 30 and 30A in figs. 14-16), the substrate having an upper and lower surface, the upper surface having conductors (portion connected with solder balls 36 – see fig. 12; alternately, items 82 in figure 14); positioning at least one first-level semiconductor device (40 in figs. 6-7; 130 in figs. 12-13; 30/30A in figs. 14-16) within the receptacle, the backside of the device being substantially coplanar with the lower surface of the substrate (figures 6-7 and 12-13) or located within a plane extending through the substrate (figs. 14-16), an interstitial space remaining at least between peripheral edges of the device and the substrate (figures 6-16); positioning a second level device (30 in figs. 6-7; 140 in figs. 12-13; 40 in figs. 14-16) above the upper surface of the substrate, a portion of the device superimposed with the upper surface of the substrate (see figures 6-16); electrically connecting the first level semiconductor device to the conductors on the upper surface of the substrate by first level conductive members at least partially carried by the second level device (first level device is connected to the substrate through the solder balls between the first and second devices, the circuitry on the second level device, and the solder balls between the second level device and the interposer; also see column 4, lines 20-65; column 5, lines 20-40); and electrically connecting the second level device to the conductors on the upper surface of the substrate by second level conductive members (solder balls between interposer 32 and the upper substrate), wherein connecting the first and second devices to the interposer includes positioning intermediate conductive elements (solder balls) between bond pads and conductors of the interposer (column 4, lines 1-10).

Regarding claims 2-4, Bertin discloses introducing encapsulant material (34, 96) into the receptacle to fill a portion of the interstitial space (figure 10) after the step of electrically

connecting the first device to the substrate (see figures 9 – where connection is completed and 10 – where encapsulant is dispensed), and introducing encapsulant between the second level device and the first level device (figure 10 – also see column 4, line 64 – column 5, line 5).

Regarding claims 7 and 8, Bertin discloses positioning the second level device in a flip chip arrangement over the first level device and the interposer (figures 6, 7, and 14-16), wherein the first level device and second level device are secured to one another before positioning the second level device (column 4, lines 40-65).

Regarding claims 9 and 10, Bertin discloses providing a multi-interposer substrate on which the first and second device are positioned, and singulating individual assemblies from the multi-interposer substrate (column 5, lines 5-15; figures 12-13).

Regarding claims 13-17, Bertin discloses positioning another first level device (30A) within the receptacle, where a backside of the another first level device faces the backside of the first level device (column 5, lines 29-30) and positioning a third level device (40A) over the lower surface of the substrate (figure 14), wherein bond pads of the another first level device are connected to corresponding conductors on the lower surface of the substrate (through lower solder balls and circuitry on chip 40A; see figures 14-16; column 4, lines 20-65; column 5, lines 20-40), bond pads of the third level device are connected to bond pads of the another first level device (figures 14-16), and bond pads of the third level device are connected to conductors on the lower surface of the substrate (figures 14-16).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 7, 8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,791,195 to Urushima et al. in view of U.S. Patent Publication No. 2001/0004128 to Park et al. (cited by Applicant).

Regarding claims 1, 2, 11, and 12, Urushima discloses a method for assembling a multi-die package, comprising: providing an interposer (48) having a substantially planar substrate (figure 11a) and a receptacle (51) formed substantially through the substrate (figure 11a), the substrate having upper and lower surfaces with conductors (35) on the upper surface (figure 11a); positioning at least one first-level device (3d) within the receptacle, an interstitial space remaining between peripheral edges of the device and substrate (figure 11a; a portion of 51 remains between device 3d and interposer 48); positioning a second level device (3c) above the upper surface of the substrate (figure 11a), a portion of the second level device superimposed with the upper surface of the substrate (figure 11a- device 3c clearly is disposed on and partially overlaps the interposer); electrically connecting the first level device to the conductors on the upper surface of the substrate by first-level conductive members at least partially carried by the second level device (device 3d must be connected to the substrate through ball bumps 21 as well as circuitry on the second device – see figure 11a), and electrically connecting the second device

to the conductors on the upper surface of the substrate by second level conductive members (through bumps 21 carried by the second level device 3d between the device and the interposer).

Since the deviation in planarity between the bottom surface of the interposer and the backside of the chip is quite small, they are considered to be "substantially" coplanar (see fig. 11a).

However, assuming arguendo, Urushima does not specifically disclose that the backside of the first level device is substantially coplanar with the lower surface of the substrate.

Park discloses adhering a film (50; paragraph 0054) to the lower surface of a substrate (10) to cover a portion of the receptacle prior to placing the first level device (2) therein (figures 2A-2B, applying an encapsulant material (40 – figure 2E; paragraph 0059), and then removing the adhered film following curing (paragraph 0059) of the encapsulant material (figure 2G; paragraph 0061), such that the backside of the first level device is coplanar with the lower surface of the substrate (paragraph 0017; figures 2A-2G).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the bottom adhesive film in Park to the interposer structure of Urushima, such that the bottom surfaces of the interposer and first level device are coplanar. The rationale is as follows: A person having ordinary skill in the art would have been motivated to apply an adhesive film to the bottom of the substrate, apply encapsulant, and remove the film, because doing so precisely controls the position of the first level semiconductor device, provides protection for the active surface of the chip, controls the flow of encapsulant, leaves the bottom surface of the chip exposed for improved heat dissipation, and provides a lower profile for the packaged assembly (see Park, paragraphs 0016-0018 and 0021).

Regarding claim 7, Urushima discloses positioning the second level device in a flip-chip arrangement over the first level device; and positioning the second level device over the interposer (figure 11a).

Regarding claim 8, Urushima discloses securing the first and second level devices to one another before positioning the second device (figure 11b; column 20, lines 10-30).

6. Claims 18-22 are rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,441,495 to Oka et al. or, in the alternative, under 35 U.S.C. 103(a) as obvious over Oka et al. in view of U.S. Patent No. 5,841,191 to Chia et al.

Regarding claim 18, Oka discloses providing an interposer with a substantially planar substrate (1a; figure 17, 18, 20, 23) and a receptacle formed substantially through the substrate (12a); positioning a first device (2c) over a first surface of the interposer, at least one bond pad (23, 24) being exposed to the receptacle (figure 17); positioning a second device (2d) over a second surface of the interposer, at least one bond pad (22a) being exposed to the receptacle (figure 17); and electrically connecting the bond pads through the receptacle (figure 17; column 13, lines 15-55). Oka further indicates that the substrate is a lead frame formed of a ribbon of metal (column 6, lines 6-10) or a synthetic resin (column 9, lines 59-60), and thus is considered to include both rigid and flexible embodiments. Additionally, since many embodiments in Oka require wirebonding between the chip and the substrate, the substrate must be substantially rigid to prevent breakage of the wirebonds. Hence, Oka is reasonably construed as disclosing a "substantially rigid substrate."

Oka, however, does not specifically teach that the substrate is rigid.

Chia teaches that a tape-type substrate used for tape automated bonding is preferably a rigid tape substrate (column 1, lines 18-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the substrate in Oka is rigid, as suggested by Chia. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a rigid substrate, because Chia shows that a rigid substrate is preferred for tape automated bonding between a tape substrate and a chip (Chia, column 1, lines 18-24), and Oka indicates that the substrate, which may be rigid or non-rigid (see Oka, column 6, lines 6-10 and column 9, lines 59-60) is used in a tape automated bonding process (Oka, column 13, lines 16-55).

Regarding claims 19 and 21, Oka discloses that conductive structures 22a and 23 are secured to the bond pad of the opposite chip after positioning (column 13, lines 15-55).

Regarding claim 20, Oka discloses that the conductive structures 22a, 23, and 24 are secured to the bond pad of their respective chips (2D and 2C, respectively) before positioning (see column 13, lines 15-55).

Regarding claim 22, Oka discloses that the first device comprises a portion of a redistribution circuit (see column 13, lines 55-67; figures 17-18).

Response to Arguments

7. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new grounds of rejection.

Insofar as the arguments can be applied to the present rejections, they are addressed as follows:

Regarding Oka, the Applicant argues that Oka discloses the use of polymeric tape, which is not substantially rigid. The Examiner notes that the specification does not provide any indication as to the metes and bounds of "substantially rigid." Hence, the Examiner assumes that "substantially rigid" would encompass any substrate with sufficient rigidity to support a wirebond without breakage occurring due to substrate flexing. Since Oka discloses that a wirebonds are supported by the assembly, and since Oka indicates that the substrate may be formed of metal, the Examiner considers the substrate in Oka to reasonably be construed as "substantially rigid." Nonetheless, an additional reference has been applied to indicate use of a rigid substrate with a TAB process. The Examiner notes that in the only embodiment of the Applicant's disclosure including the first device over one surface of the interposer and a second device over the second surface of the interposer with the devices connected through a receptacle in the interposer (Applicant's figure 9 embodiment), the substrate is described as a flex substrate and not a rigid substrate (Applicant's disclosure, paragraph 0078).

Additionally, the Applicant argues that Oka does not teach a redistribution circuit on the first chip. The Examiner, however, maintains that the circuitry connecting the second chip 2D to the terminal portions 15 through the electrodes 22A, 23, and 24, as well as through wiring on the chip 2C constitutes a redistribution circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
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jmd

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